CLAIMS:

1. A memory card comprising a non-volatile memory, and a memory controller for controlling operation of said non-volatile memory, wherein

said memory controller is capable of interfacing with outside according to a predetermined protocol;

said memory controller controls, in a memory control in response to an access instruction from outside, a process for adding an error correction code to data which is written to said non-volatile memory from outside, or a process for conducting an error detection and correction process, by using said error correction code, to data which is read out from said non-volatile memory to outside; and

said memory controller controls a process for conducting an error detection and correction process to memory information of said non-volatile memory by using said error correction code independently of said process in response to the access instruction from outside.

2. A memory card according to claim 1, wherein said memory controller comprises operation control means for instructing the error detection and correction process at predetermined time intervals independently of said process in response to the access instruction from outside.

3. A memory card according to claim 1, wherein

said memory controller comprises operation control means for instructing the error detection and correction process independently of said process in response to the access instruction from outside, in response to connection of electric power supply to said memory card.

4. A memory card according to claim 1, wherein said memory controller comprises operation control means for changing a memory area for error-corrected memory information when a number of error generation times exceeds a predetermined number of times, in the error detection and correction process independently of the process in response to the access instruction from outside.

5. A memory card according to claim 1, wherein said memory controller comprises operation control means for changing a memory area for error-corrected memory information when a number of error generated bits exceeds a predetermined number of bits, in the error detection and correction process independently of the process in response to the access instruction from outside.

6. A memory card according to claim 4, wherein said non-volatile memory includes, as an information memory area, a data area, a substitution area for substituting for a defect portion of said data area, substitution managing area for defining correspondence between said data area and said substitution

area, and a parameter area; and

said operation control means obtains information of said predetermined number of times from said parameter area, and changes the memory area of said error-corrected memory information to said substitution area.

7. A memory card according to claim 5, wherein

said non-volatile memory includes, as an information memory area, a data area, a substitution area for substituting for a defect portion of said data area, substitution managing area for defining correspondence between said data area and said substitution area, and a parameter area; and

said operation control means obtains information of said predetermined number of bits from said parameter area, and changes the memory area of said error-corrected memory information to said substitution area.

8. A memory card according to claim 4, wherein

said non-volatile memory includes, as an information memory area, a data area, a substitution area for substituting for a defect portion of said data area, substitution managing area for defining correspondence between said data area and said substitution area, and a parameter area; and

said operation control means records the number of error generation times generated in said error detection and correction process in a correspond-

ing data area in said non-volatile memory, and changes the memory area of said error-corrected memory information to said substitution area.

9. A memory card according to claim 2, wherein said operation control means is a program-controlled data processor.

10. A memory controller comprising:

a host interface circuit capable of conducting input and output operation according to a predetermined protocol;

a memory interface circuit connectable to a non-volatile memory; and

a control circuit connected to said host interface circuit and said memory interface circuit, wherein

said control circuit is capable of controlling a first process of outputting data, which is obtained by adding an error correction code to write-data inputted from said host interface circuit, together with write-control information from said memory interface circuit, a second process of outputting data, which is obtained by applying an error detection and correction process to read-data inputted to said memory interface circuit, from said host interface circuit according to read-control information outputted from said memory interface circuit, and a third process of outputting data, which is obtained by applying an error detection and correction process to

the read-data inputted to said memory interface circuit, together with the write-control information from said memory interface circuit according to the read-control information outputted from said memory interface circuit.

11. A memory controller according to claim 10, wherein said control circuit includes operation control means for instructing said third process to be carried out at predetermined time intervals.

12. A memory controller according to claim 10, wherein said control circuit includes operation control means for instructing said third process to be carried out in response to connection of electric power supply to said memory controller.

13. A memory controller according to claim 11, wherein said operation control means instructs to output write-control information for changing a memory area for error-corrected read-data when a number of error generation times exceeds a predetermined number of times, in said third process.

14. A memory controller according to claim 11, wherein said operation control means instructs to output write-control information for changing a memory area for error-corrected read-data when a number of error generated bits exceeds a predetermined number of bits, in said third process.

15. A memory controller according to claim 13, wherein said operation control means inputs information

of said predetermined number of times from said memory interface circuit when said memory interface circuit inputs said read-data.

16. A memory controller according to claim 14, wherein said operation control means inputs information of said predetermined number of bits from said memory interface circuit when said memory interface circuit inputs said read-data.

17. A memory controller according to claim 13, wherein said operation control means instructs to output the number of error generation times, which is produced in the error detection and correction in each of said second and third processes, together with said write-control information from said memory interface circuit.

18. A memory controller according to claim 10, wherein said control circuit includes an ECC circuit used for generation of said error correction code and said error detection and correction.